14-12-24

Printing Pages : 1 Paper Code : - KCSE-302 (B) (SVSU) : 2024-2025/R

Enrollment No. | | | | | | | | | | | | | |

B.TECH. (CSE/IT)
II YEAR, III SEMESTER EXAMINATION
COMPUTER ORGANISATION AND ARCHITECTURE

[Time : 03:00 Hours] [Max. Marks : 70]

NOTE:- ATTEMPT ALL THE QUESTIONS AS PER GIVEN INSTRUCTIONS.

QUESTION NO.-1: ATTEMPT ANY FOUR PARTS. (4*3=12)

a) What do you understand by bus arbitration? Discuss in detail.
b) What is Stack? Explain the working of PUSH and POP operations?
c) What is Input Output Subsystem?
d) What is programmed initiated input output?
e) What is interrupt initiated input output?
f) What do you understand by parallel processing? Also discuss advantages and disadvantages

QUESTION NO.-2: ATTEMPT ANY THREE PARTS. (3*4=12)

a) Explain memory hierarchy with description of semiconductor memory?
b) What are the differences between hardwired and microprogrammed control unit?
c) Explain the working and action of DMA with the help of a suitable example.
d) Explain types of register in computer organization and architecture

QUESTION NO.-3: ATTEMPT ANY THREE PARTS. (3*6=18)

a) What is a three-state buffer? How it can be used in bus system?
b) Explain the process of binary division with the help of a suitable example.
c) Discuss the concept of virtual memory in computer organization.
d) Give the main physical differences between the following memory technologies: SRAMs, flash memories and CD-ROM.?

QUESTION NO.-4: ATTEMPT ANY TWO PARTS. (2*7=14)

a) Using BOOTHs algorithm multiply 23(Multiplicand) by 29(Multiplier), each no .is represented by 6 bit?
b) Discuss four segment instruction pipeline with the help of flow chart, in detail.
c) Draw the neat sketch of memory hierarchy and explain the need of cache memory

QUESTION NO.-5: ATTEMPT ANY TWO PARTS. (2*7=14)

a) Explain pipeline and performance measures.
b) Explain the following
i) Memory mapped I/O
ii) I/O Registers
iii) Hardware Interrupts
c) What are various cache mapping techniques? Explain all with example. Differentiate among all mapping techniques.

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12-12-24

ting Pages : 2 Paper Code : BECE-306 (A) (SVSU) : 2021-2022/R

Enrollment No.

B.TECH (CS/IT,CSE-AI-ML)
II[nd] YEAR, III SEM. EXAMINATION
DIGITAL ELECTRONICS

Time : 3:00 Hours] [Max. Marks : 70]

Note: Attempt all questions as per instructions.

Long Question : Answer Any Three [10×3=30]

Explain the circuit and functioning of full and half Subtractors.

What are the classifications of Logic Families? Explain the difference between TTL and CMOS.

Define Bistable Vibrator. Discuss the S-R flip flop in detail.

Differentiate between multiplexer and demultiplexer. Explain the working of 4 X 1 MUX and 1 X 4 DEMUX.

Differentiate between combinational circuit and sequential circuit. Explain the functionality of Half adder in detail.

Short Question: Answer any Five [5×5=25]

Differentiate between Encoders and decoders with suitable examples.

Explain the ECL logic family.

Define logic gates? What are the types of Logic gates? Explain the EXNOR gate and its truth table.

What is shift registers? Explain the working of SIPO with suitable examples.

Explain the VLSI Design Flow.

Explain the Parallel Adder. In how many ways we can implement it. Discuss with suitable examples.

Differetiate between implicants, prime implicants and essential implicants with suitable example.

Objectives Question: Answer All Question [15×1=15]

Which of the following is considered as Sequential Circuit?
a) Encoder
b) Multiplexer
c) Flip Flop
d) Half subtractor

Complement of the expression 0001 is _____
a) 0001
b) 1001
c) 1110
d) 0110

Which gate is also known as MODULE 2 SUM?
a) Exor
b) Exnor
c) AND
d) NOR

The prime implicant which has at least one element that is not present in any other implicant is known as _____
a) Complement b) Essential Prime Implicant c) Prime Complement d) Implicant

[P.T.O.]

hich of the following is correct?
In BCD, each digit is represented by 4 bit binary no.
Excess- 3 code is unweighted code which is self-complementing.
Can't determined
) All of the above

here are 2 outputs for half adder one is sum and other is carry then The Sum output of Half adder is
)A+B
)A'B+AB'
)A'B'+AB
)0

How many NAND gates are needed to implement half adder?
a) 5
b) 4
c) 3
d) 2

SSI stands for:
a) Small scale integration
b) Ultra-very large scale integration
c) Very large scale integration
d) Medium large scale integration

Find the octal equivalent of (0.345)10:
a) (0.3450)8
b) (0.26050)8
c) (2.4)8
d) (91.44)8

Find the binary equivalent of $(37.55)_8$
a) $(011\ 111.\ 101101)_2$ b) $(111\ 011.\ 101100)_2$ c) $(011.100101)_2$ d)$(111.101100)_2$

A counter which counts from 0 to 5 is called?
a) Mod -6 counter b) Mod- 5 counter c) Mod -4 counter d) Mod – 7 counter

Find the invalid statement in terms of complement?
a) Complements are used in digital computer to simplify the subtraction operation.
b) The complement formula is r^n – N where r is radix, n is no of digits and N is given number
c) The 1's complement of 1011 is 0101.
d) All the above

PLA architecture is
a) Programmable AND and Fixed OR
b) Programmable AND and Programmable OR
c) Fixed AND and ProgrammableOR
d) Fixed AND and Fixed OR

4. Which number system has a base 16
a)Hexadecimal b)Octal c)Binary d)Decimal

5. If there are 10 bits to store then how many flip flops are required?
a) 10 b) 11 c) 12 d) 9

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